Docket: 740819-653

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re New Patent Application of	)	
Keiichi FUJIMOTO et al.	)	
Japanese Priority Application No. 2001-028597	)	Attn: Applications
Japanese Priority Date: February 5, 2001	)	Branch
For: SEMICONDUCTOR INTEGRATED	)	
CIRCUIT TESTING SYSTEM AND	)	
METHOD	)	Date: September 28, 2001

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with the provisions of 37 C.F.R. 1.56 and 37 C.F.R. 1.97-1.99, it is requested that the reference listed on the attached Form PTO-1449 be made of record in the above-identified application.

A copy of this reference is submitted herewith in accordance with 37 C.F.R. 1.98(a).

Respectfully submitted,

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